

# FIG. 1

## PRINCIPLE DIAGRAM OF PRESENT INVENTION

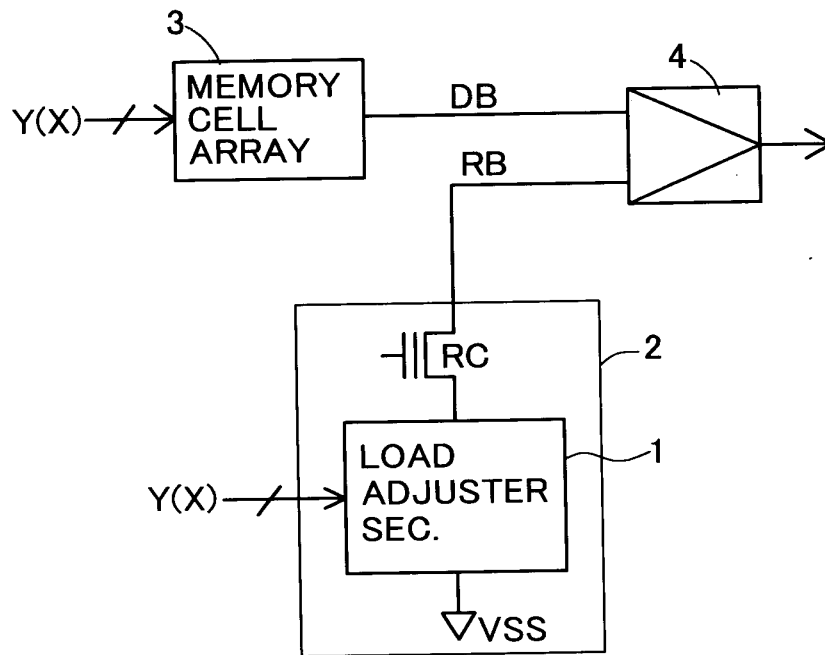


FIG. 2 CIRCUIT DIAGRAM OF FIRST EMBODIMENT

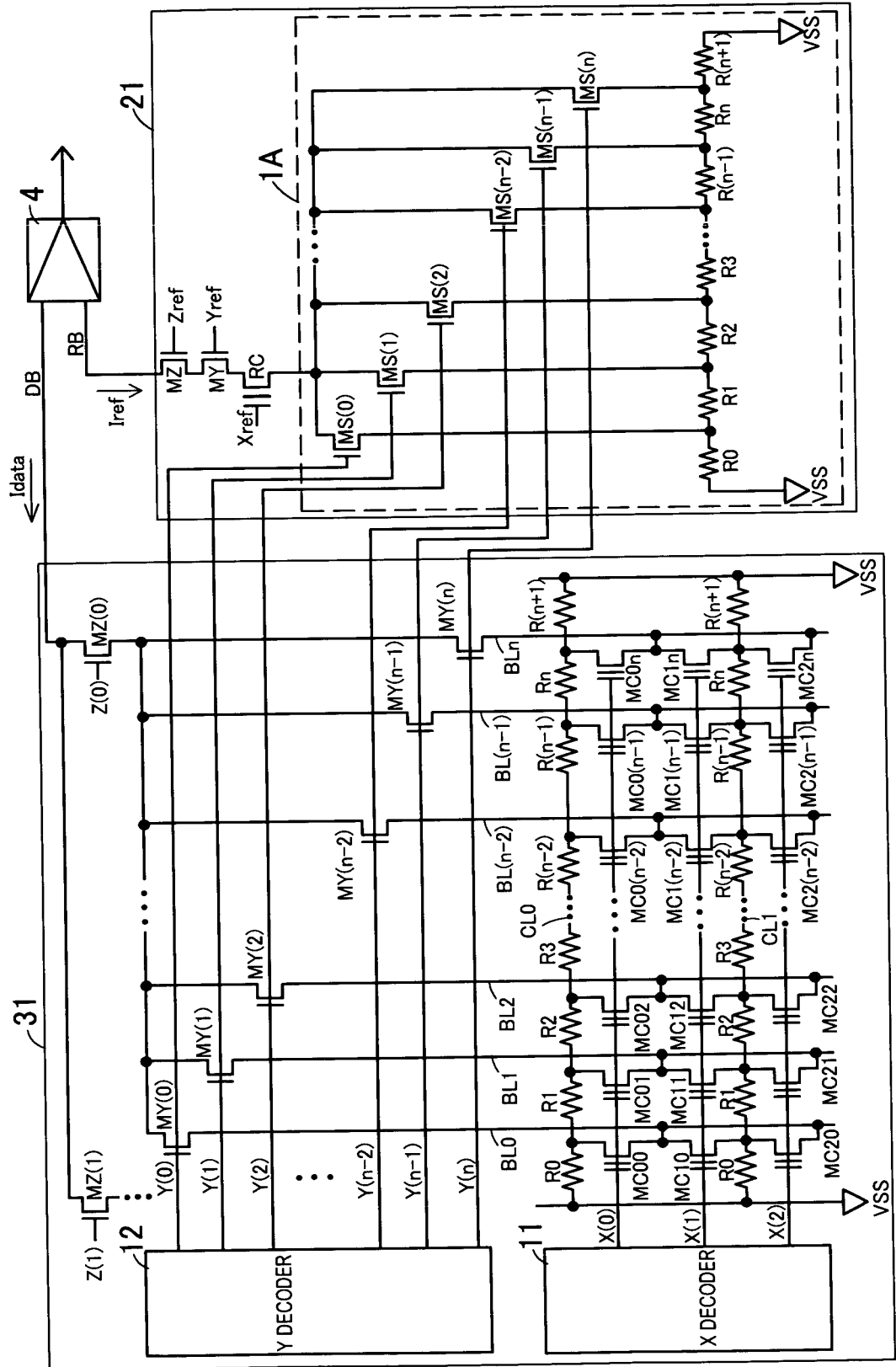
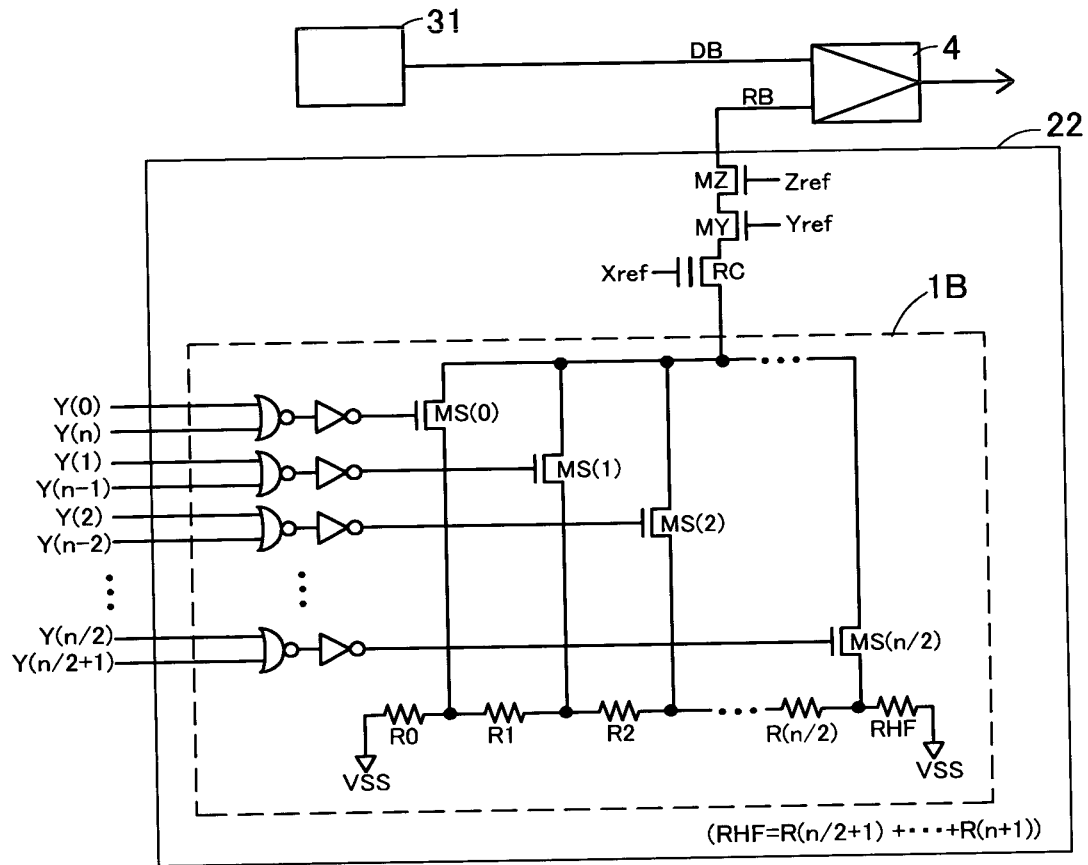


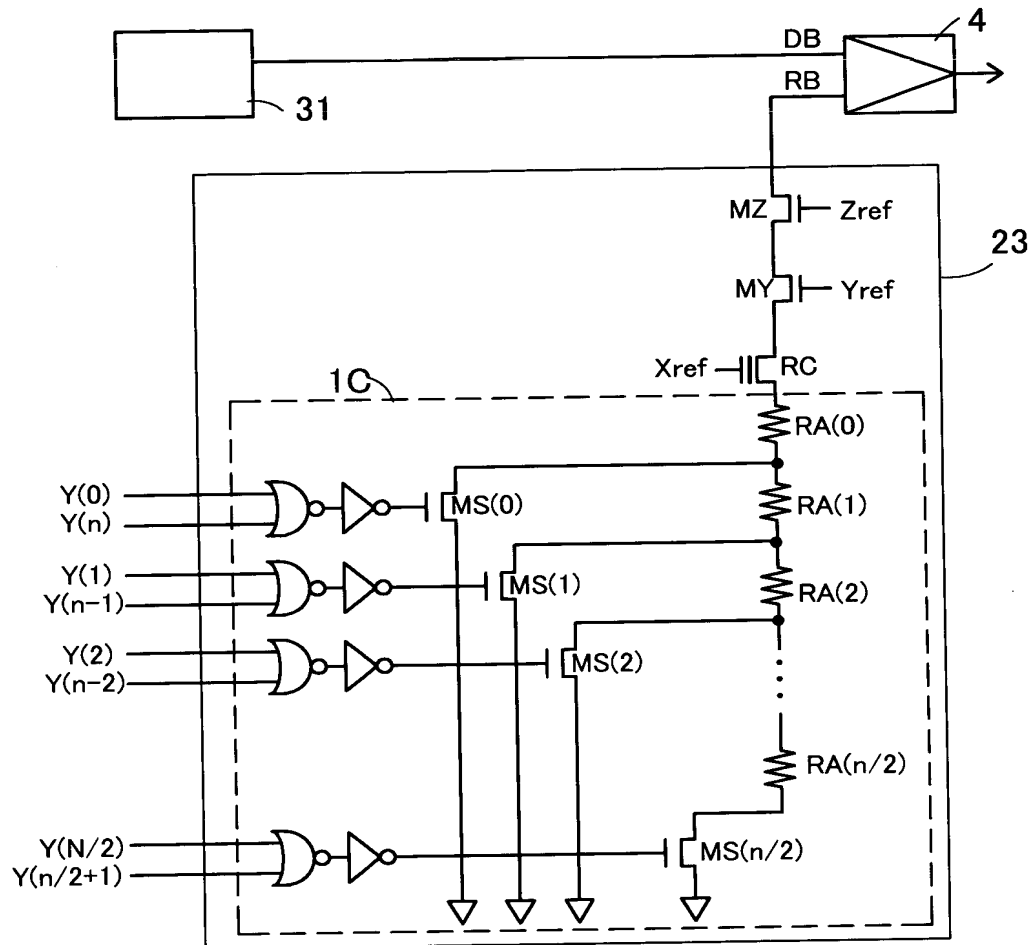
FIG. 3

CIRCUIT DIAGRAM OF SECOND EMBODIMENT



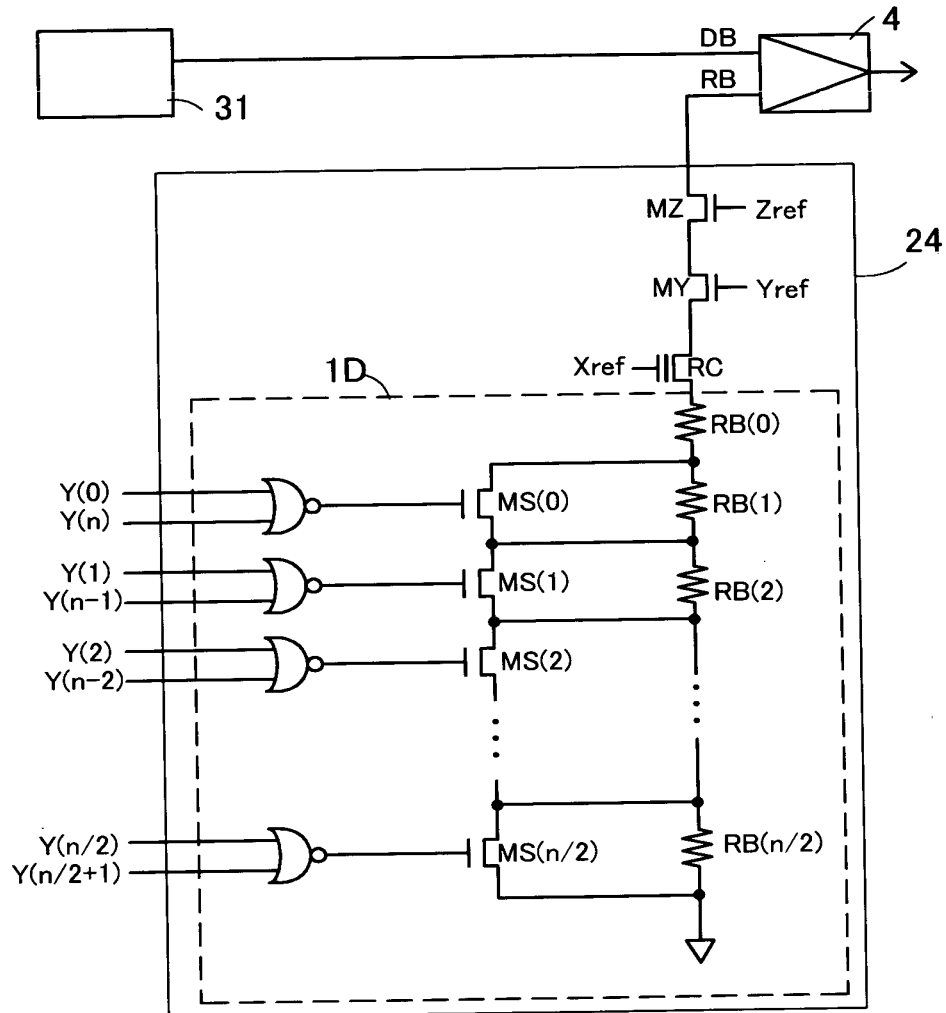
# FIG. 4

CIRCUIT DIAGRAM OF THIRD EMBODIMENT



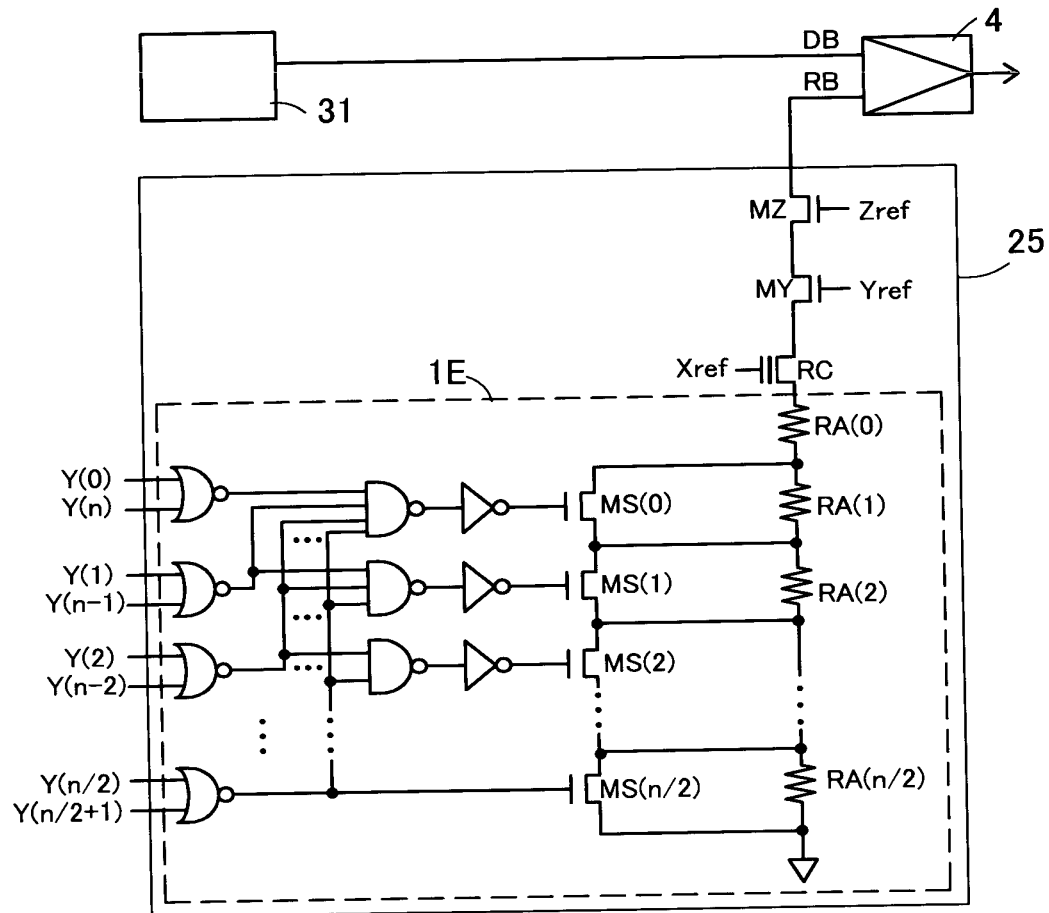
# FIG. 5

CIRCUIT DIAGRAM OF FOURTH EMBODIMENT

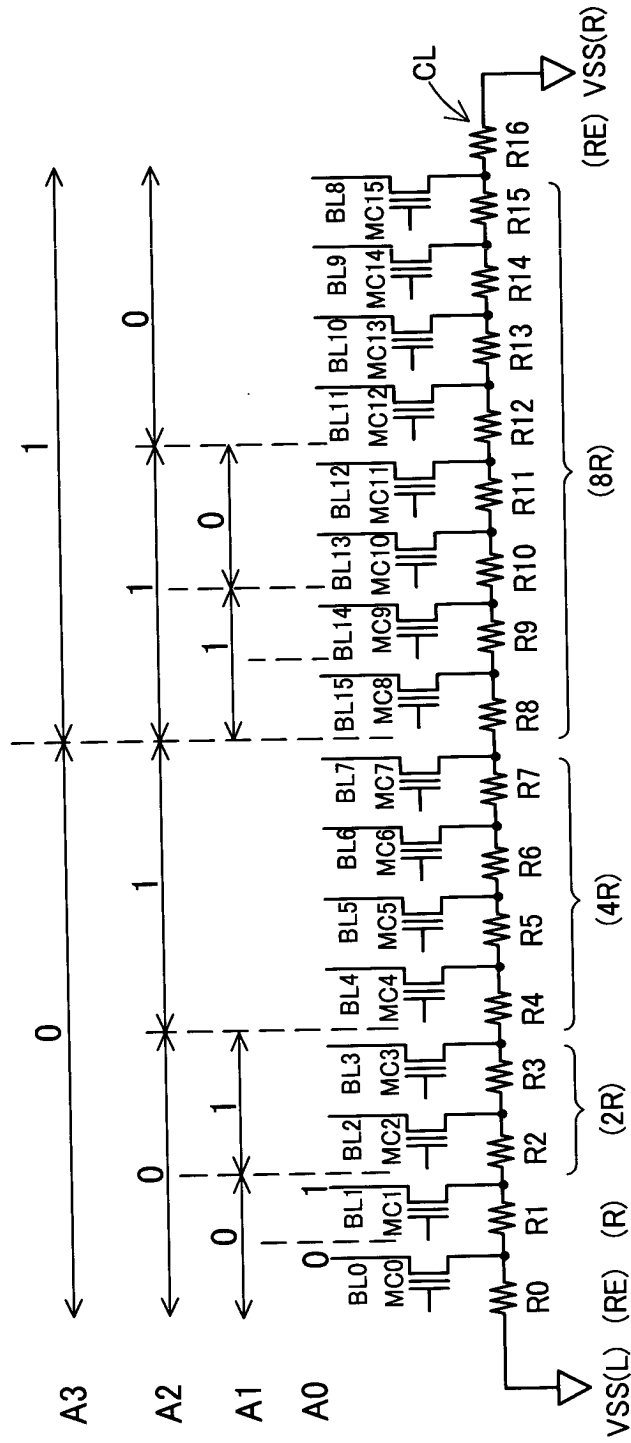


**FIG. 6**

**CIRCUIT DIAGRAM OF FIFTH EMBODIMENT**

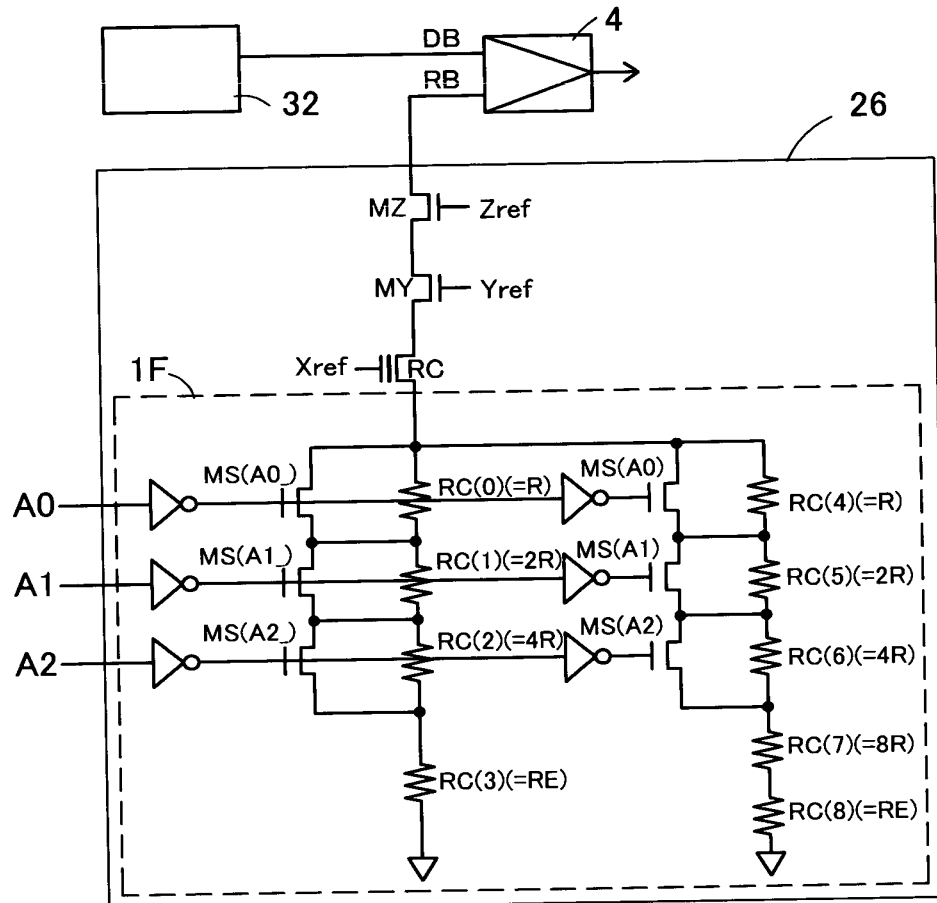


**FIG. 7**  
 SCHEMATIC DIAGRAM FOR ILLUSTRATING COLUMN-DIRECTION  
 ADDRESSING IN MEMORY CELL ARRAY OF SIXTH EMBODIMENT



**FIG. 8**

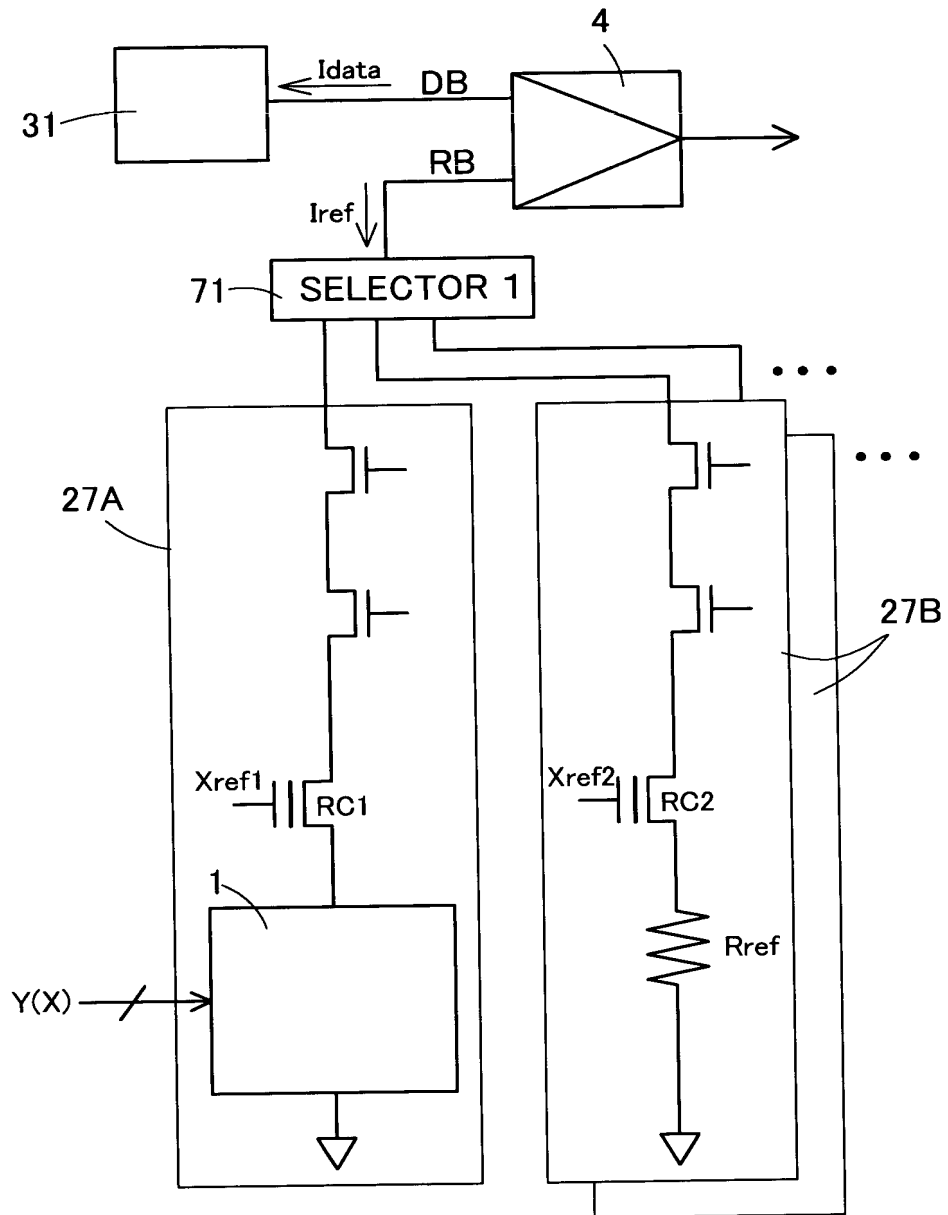
**CIRCUIT DIAGRAM OF SIXTH EMBODIMENT**





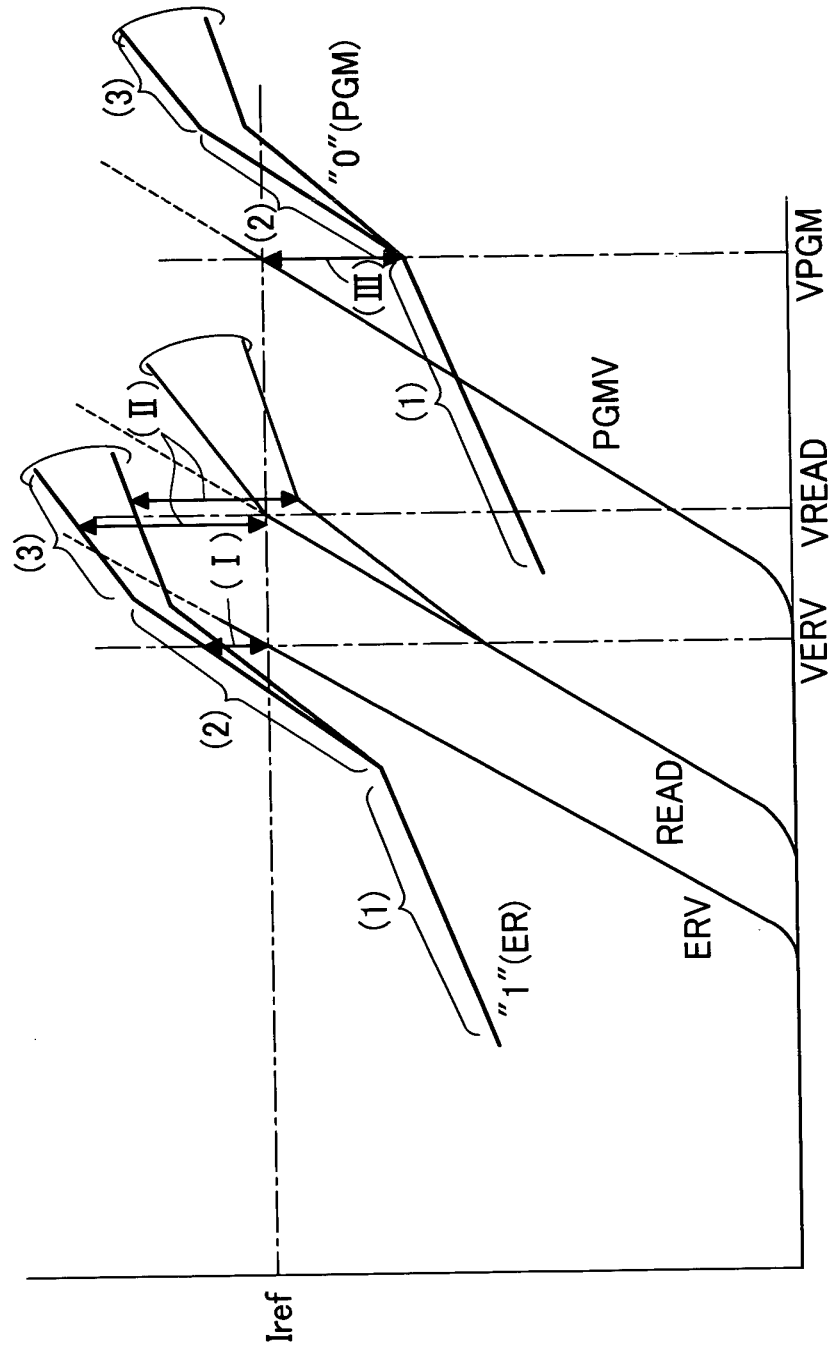
**FIG. 9**

CIRCUIT BLOCK DIAGRAM OF SEVENTH EMBODIMENT



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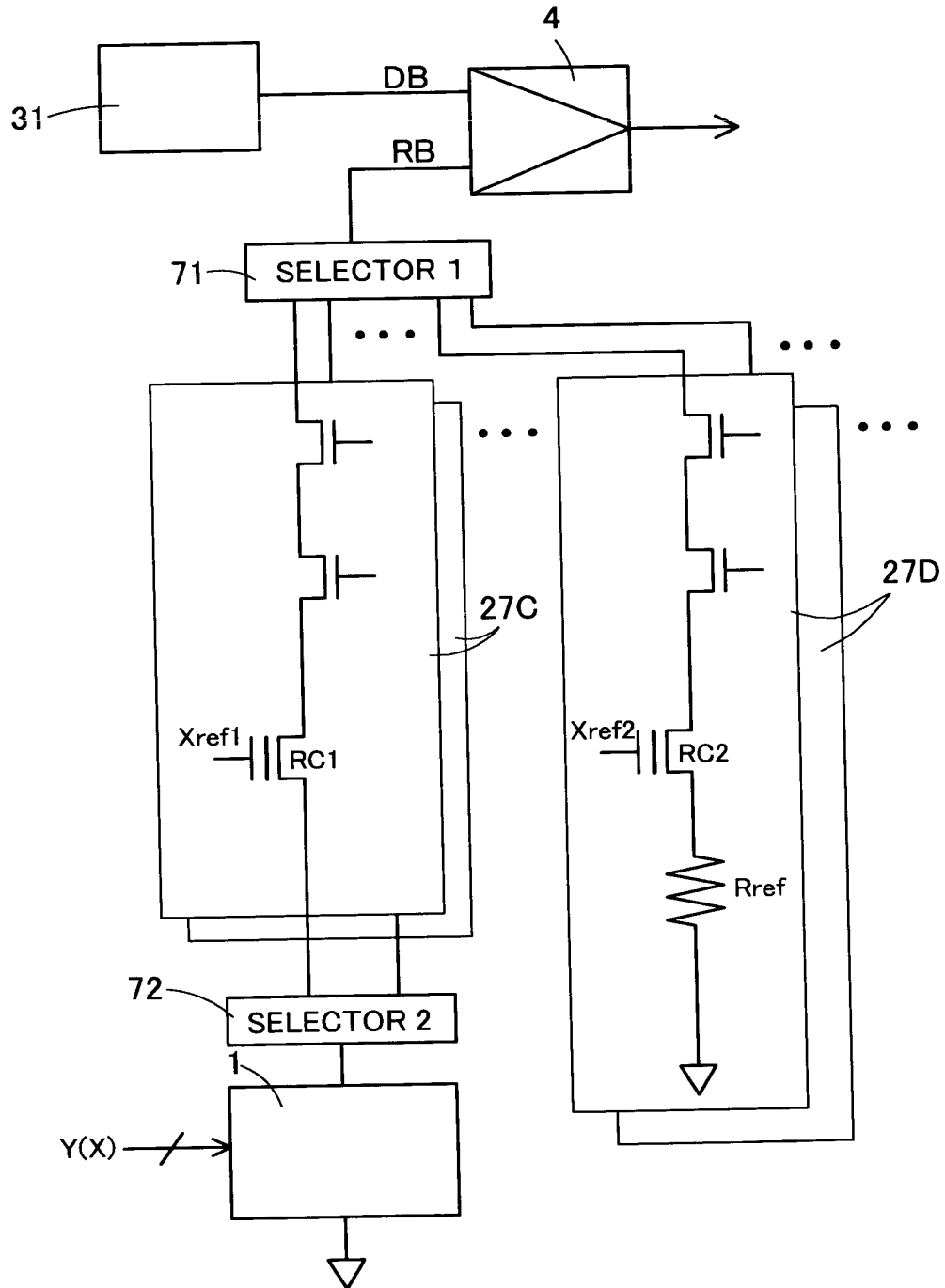
**FIG. 10**  
 TRANSISTOR CHARACTERISTIC OF SEVENTH EMBODIMENT



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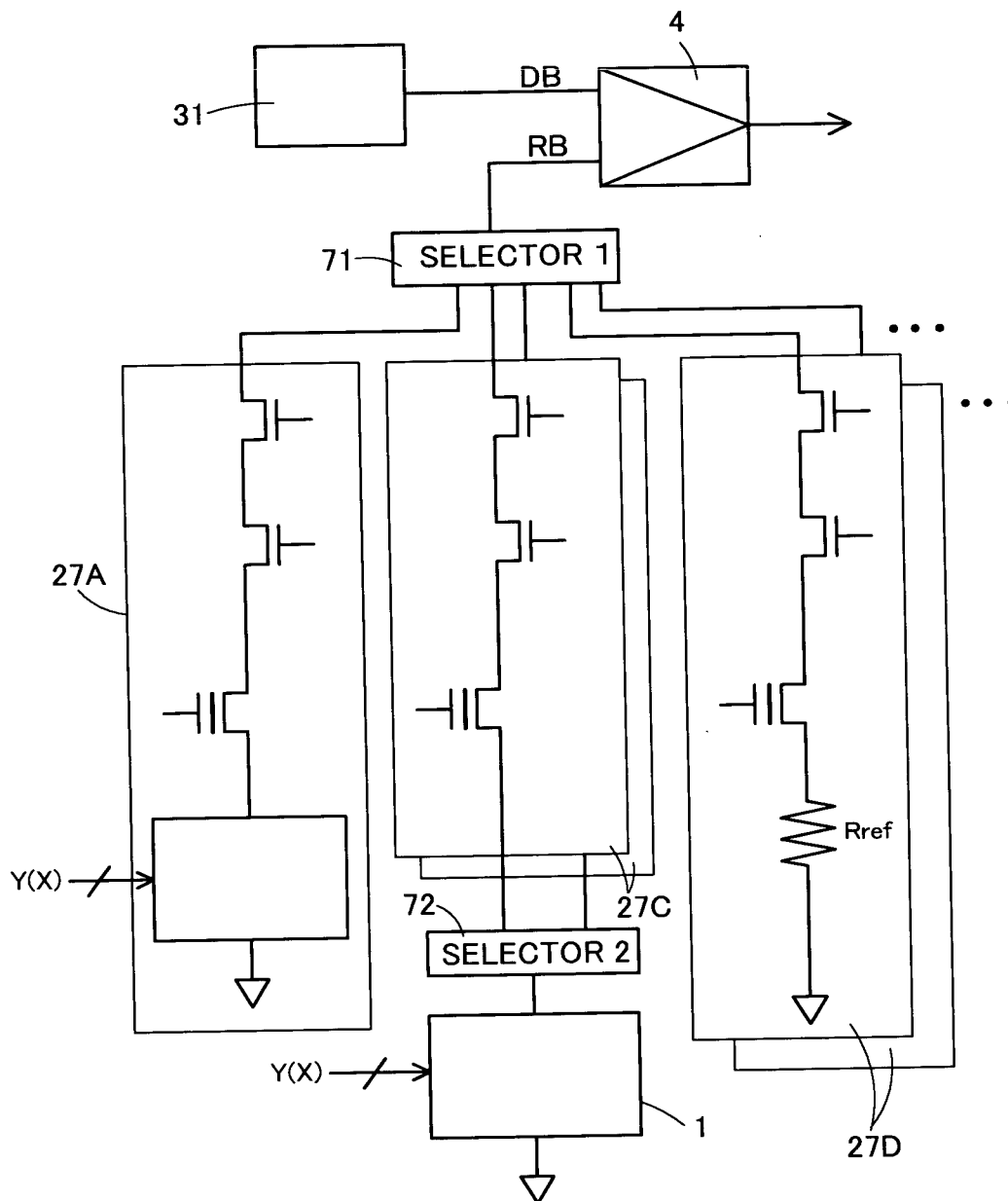
# FIG. 11

FIRST VARIANT DIRECTED TO SEVENTH EMBODIMENT



## FIG. 12

SECOND VARIANT DIRECTED TO SEVENTH EMBODIMENT



**FIG. 13**

**CIRCUIT BLOCK DIAGRAM OF EIGHTH EMBODIMENT**

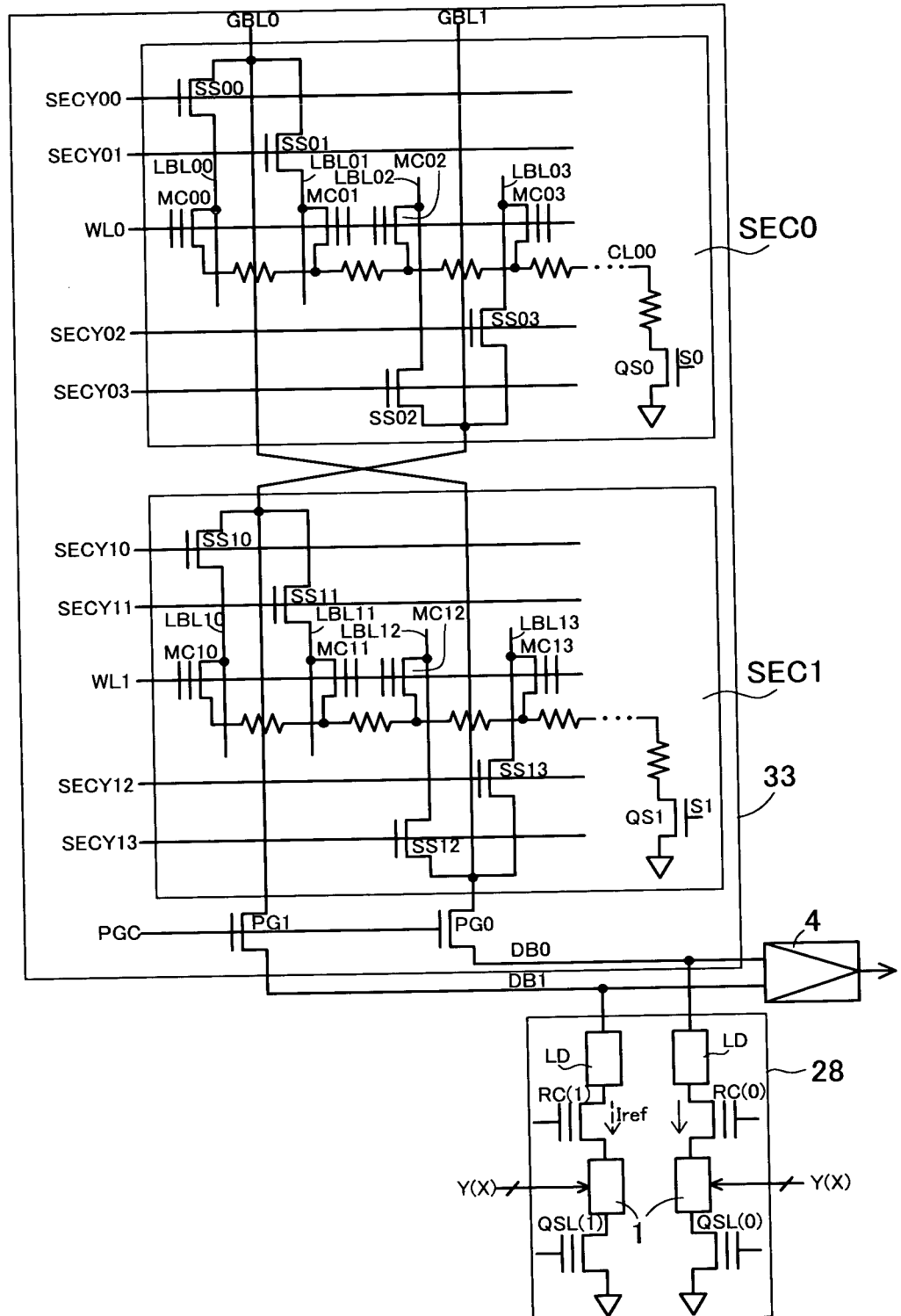




FIG. 15

CIRCUIT BLOCK DIAGRAM OF VARIANT DIRECTED TO EIGHTH EMBODIMENT

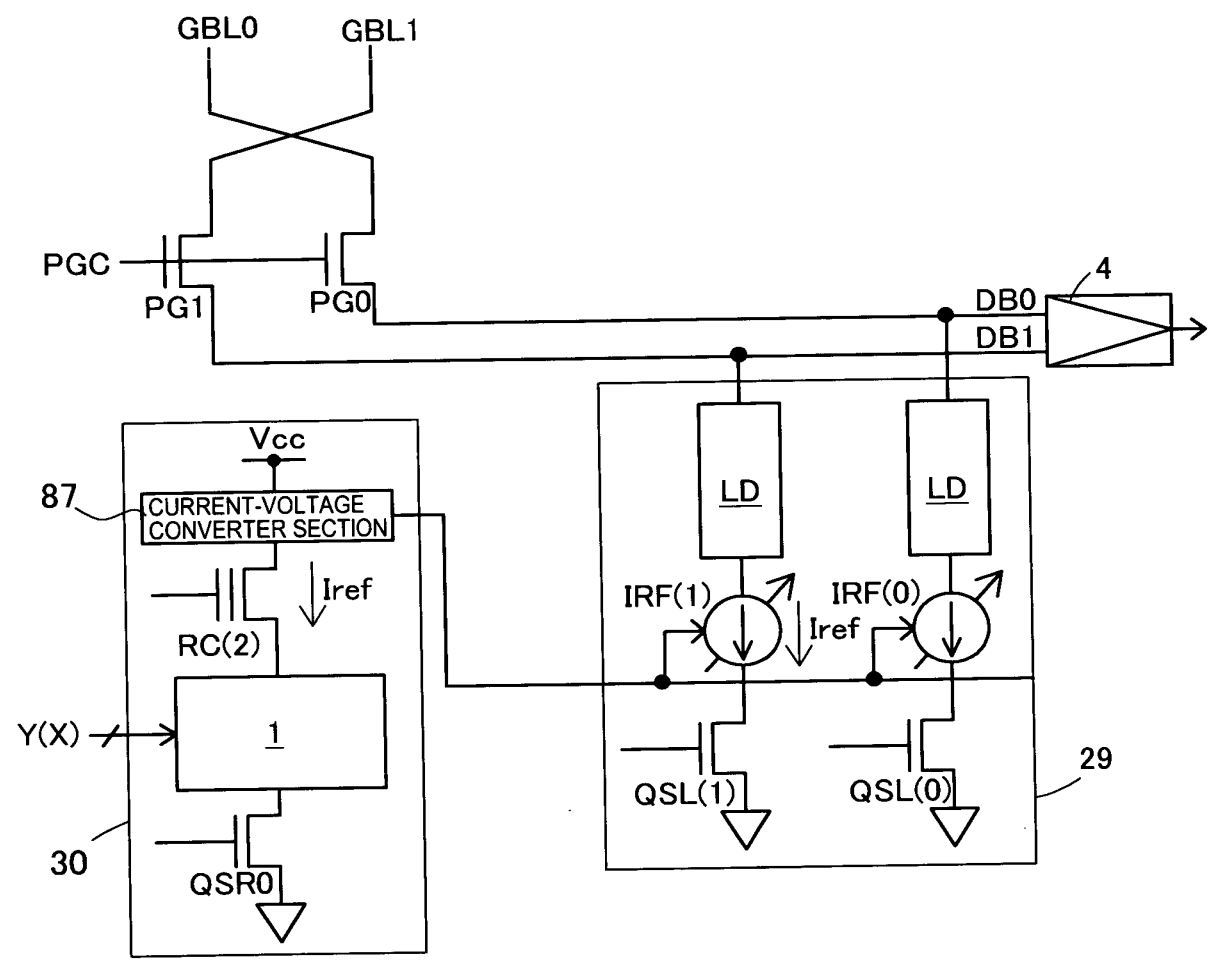
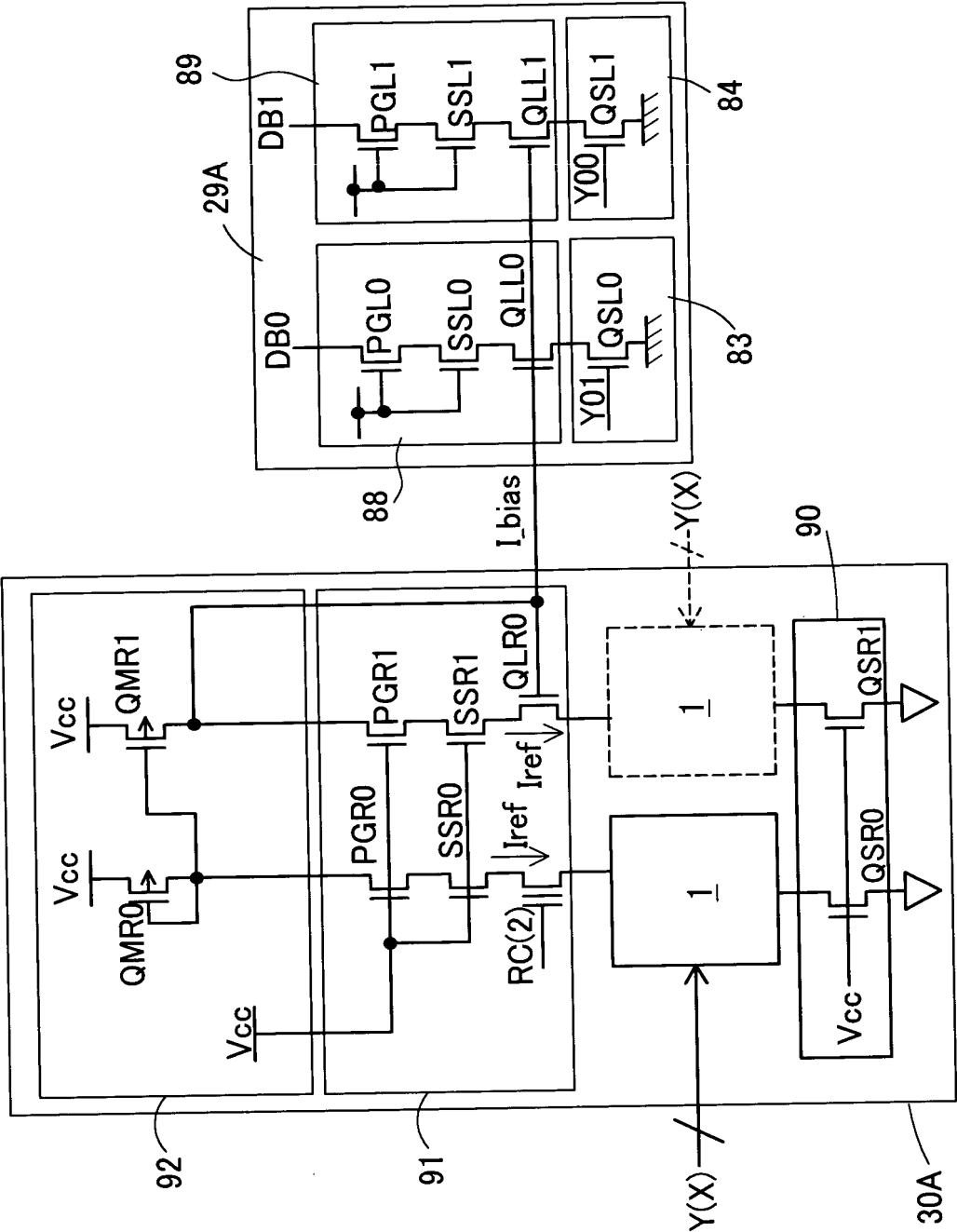
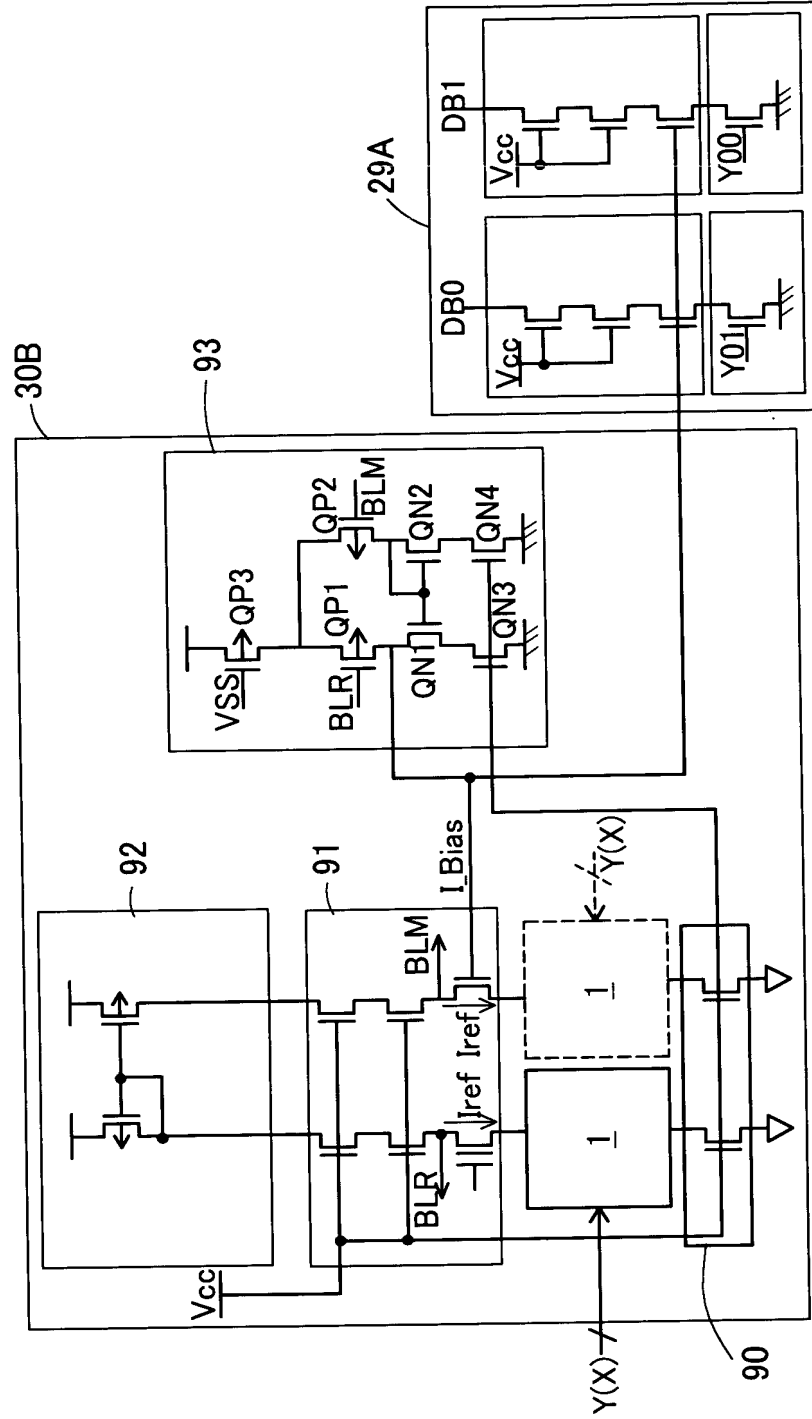


FIG. 16  
FIRST SPECIFIC EXAMPLE OF VARIANT DIRECTED TO EIGHTH EMBODIMENT







# FIG. 18 PRIOR ART

## CONVENTIONAL REFERENCE SECTION

